Notice of Allowability	Application No. 09/347,409	Applicant(s) AKIMOTO ET AL.	
	Examiner Herng-der Day	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendments received 10/19/04 and 6/24/05*.

2. ☒ The allowed claim(s) is/are *4, 6, 10, and 12, now renumbered as 1-4*.

3. ☒ The drawings filed on *01 April 2003* are accepted by the Examiner.

4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *06242005* .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This communication is in response to Applicants' Amendment to Office Action dated February 18, 2004, mailed October 19, 2004, Applicants' RCE to Office Action dated February 16, 2005, mailed March 18, 2005, and Applicants' Amendment faxed June 24, 2005.

1-1. Claims 15-16 have been added. Claims 2-4, 6, 8, 10, and 13 have been amended. Claims 2-3, 5, 8-9, 11, and 13-16 have been cancelled. Claims 4, 6, 10, and 12 are pending.

1-2. Claims 4, 6, 10, and 12 have been examined and allowed.

Reasons for Allowance

2. The following is an Examiner's statement of reasons for allowance:

2-1. The closest prior art of record discloses:

(1) A hot-carrier-delay-degradation estimation method (Iwanishi et al., U.S. Patent 6,047,247).

(2) A hot carrier effect simulation for integrated circuits (Fang et al., U.S. Patent 6,278,964).

(3) A method of simulating hot carrier deterioration of a P-MOS transistor (Shimizu et al., U.S. Patent 5,615,377).

2-2. Independent claim 4 is directed at a method of calculating, by the use of a computer, pin-to-pin delay time and block-to-block delay time. Although estimating the aged delay time due to hot carrier effect is obvious as disclosed in the prior art, this independent claim identifies the

distinct features of calculating aged delay time for transistors directly connected to the input pin and transistors directly connected to the output pin only according to those claimed expressions.

Because the closest prior art does not teach or suggest calculating the aged delay time by those claimed expressions for transistors directly connected to the input pin and transistors directly connected to the output pin only, claim 4 is deemed allowable.

2-3. Independent claim 6 is directed at a method of calculating, by the use of a computer, a delay time occurred to a signal passing through a logic level circuit that consists of a plurality of logic blocks. Although estimating the aged delay time due to hot carrier effect is obvious as disclosed in the prior art, this independent claim identifies the distinct features of calculating aged delay time for transistors directly connected to the input pin and transistors directly connected to the output pin only according to those claimed expressions.

Because the closest prior art does not teach or suggest calculating the aged delay time by those claimed expressions for transistors directly connected to the input pin and transistors directly connected to the output pin only, claim 6 is deemed allowable.

2-4. Independent claims 10 and 12 are computer-readable medium claims including same method limitations as in the allowable claims 4 and 6 respectively and are deemed allowable for the same reasons as claims 4 and 6.

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Herng-der Day whose telephone number is (571) 272-3777. The Examiner can normally be reached on 9:00 - 17:30. Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: (571) 272-2100.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Jean R. Homere can be reached on (571) 272-3780. The fax phone numbers for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Herng-der Day H.D.
June 24, 2005

JEAN R. HOMERE
PRIMARY EXAMINER